PTO/SB/17 (01-06)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

[X] Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 250.00

Complete if Known	
Application Number	10/648,253-Conf. #5216
Filing Date	August 27, 2003
First Named Inventor	Yuan-Jen CHAO
Examiner Name	H. T. Nguyen
Art Unit	2841
Attorney Docket No.	4459-0149P

METHOD OF PAYMENT (check all that apply)

[X] Check [ ] Credit Card [ ] Money Order [ ] None [ ] Other (please identify): _____

[ ] Deposit Account Deposit Account Number: 02-2448 Deposit Account Name: Birch, Stewart, Kolasch & Birch, LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

[ ] Charge fee(s) indicated below
[ ] Charge fee(s) indicated below, **except for the filing fee**
[X] Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17
[X] Credit any overpayments

FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - =	_____ x	_____ =	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - =	_____ x	_____ =	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	**Fee Paid ($)**
_____	_____
_____	_____

3. APPLICATION SIZE FEE

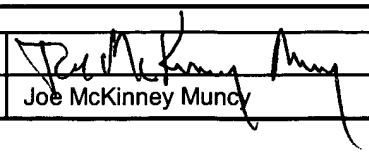
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ /50	_____ (round up to a whole number) x	_____ =	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal	250.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent)	32,334	Telephone	(703) 205-8026
Name (Print/Type)	Joe McKinney Muncy			Date	August 14, 2006

TRANSMITTAL OF APPEAL BRIEF

Docket No.
4459-0149P

In re Application of: Yuan-Jen CHAO

Application No.	Filing Date	Examiner	Group Art Unit
10/648,253-Conf. #5216	August 27, 2003	H. T. Nguyen	2841

Invention: MULTI-CHIP INTEGRATED MODULE

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: June 14, 2006 .

The fee for filing this Appeal Brief is $ 250.00 .

[ ] Large Entity [x] Small Entity

[ ] A petition for extension of time is also enclosed.

The fee for the extension of time is _____ .

[x] A check in the amount of $ 250.00 is enclosed.

[ ] Charge the amount of the fee to Deposit Account No. 02-2448 .
This sheet is submitted in duplicate.

[ ] Payment by credit card. Form PTO-2038 is attached.

[x] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 02-2448 .
This sheet is submitted in duplicate.

Dated: August 14, 2006

Joe McKinney Muncy
Attorney Reg. No. : 32,334
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8026

Docket No.: 4459-0149P
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Yuan-Jen CHAO

Application No.: 10/648,253 Confirmation No.: 5216

Filed: August 27, 2003 Art Unit: 2841

For: MULTI-CHIP INTEGRATED MODULE Examiner: H. T. Nguyen

APPEAL BRIEF

MS Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 14, 2006

Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on June 14, 2006, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Argument
VIII.	Claims Appendix A

IX. Evidence Appendix B
X. Related Proceedings Appendix C

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Gigno Technology Co., Ltd. Of Taiwan, as evidenced by the Assignment filed on August 27, 2003 at Reel 014445 and Frames 0763-0765.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 20 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: 5-8 and 17-18
2. Claims withdrawn from consideration but not canceled: None
3. Claims pending: 1-4, 9-16 and 19-26
4. Claims allowed: None
5. Claims rejected: 1-4, 9-16 and 19-26

C. Claims On Appeal

The claims on appeal are claims 1-4, 9-16 and 19-26.

IV. STATUS OF AMENDMENTS

The Amendment After Final Rejection filed on March 15, 2006, has apparently been entered according to the Advisory Action of May 3, 2006. It is noted that the Examiner has checked Box 7 but has not checked either Box a or b. However, since only Remarks were presented, it is assumed that the Amendment was entered. An Amendment was also filed on June 14, 2006. The Advisory Action of August 10, 2006 does not indicate whether the Amendment is entered or not. Only Box 7 was checked, but not Box a or b. Section 11 indicates that the new claim has been considered but is not persuasive. It is therefore assumed that the Examiner has entered the claims but still finds the claims rejected. Also, it is noted that in Section 7 the list of rejected claims includes the new claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the invention includes an integrated module having a plurality of chips including a transparent substrate 11 on which a circuit layer 110 is formed. The circuit layer 110 includes a circuit 111 for electrical inter-connection and a plurality of electrical pads 112. A plurality of first bumps 113 are formed on the electrical pads 112. The bumps can be solder, gold or copper. Chips 12 are attached to this transparent substrate 11 by way of flip-chip bonding so that the chips and the circuit 111 for electrical inter-connection form a circuit system. Second bumps 121 can be formed on the electrical pads 122 of the chip 12. A circuit substrate 13 is attached to the transparent substrate 11 which carries the chips 12. Circuit substrate 13 includes at least a circuit layer 131. Circuit layer 131 is connected to first bumps 113, so that the transparent substrate is held to the circuit substrate. A hollow portion 132 (Figure 2) is formed by this arrangement. Heat dissipation elements 14 (Figure 6) can utilize this hollow portion. A passive component 15 or active component 16 (Figure 7) can also be formed on circuit 111.

As to claim 1, the integrated module includes a transparent substrate 11, which has a circuit layer 110 formed directly on one surface. The circuit layer includes a circuit for electrical inter-connection 111 and a plurality of electrical pads 112. Two chips 12 are mounted on the transparent substrate by way of flip-chip bonding and the chips and the circuit for electrical inter-

connection form the circuit system. A circuit substrate 13 attaches to the transparent substrate and includes a circuit layer 131. The electrical pads 112 electrically connect to the circuit layer 113 of the circuit substrate.

Claim 2 depends from claim 1 and further describes the transparent substrate as a glass substrate.

Claim 3 depends from claim 1 and further describes a plurality of first bumps 113 which are formed on the electrical pads 112 to connect the electrical pads and the circuit layer of the circuit substrate.

Claim 4 depends from claim 1 and describes the plurality of second bumps 114 formed on the circuit for electrical inter-connection. The chips are electrically connected to the second bumps by way of flip-chip bonding.

Claim 9 depends from claim 1 and further describes a heat dissipation element 14 formed on the backside of at least one of the chips.

Claim 10 depends from claim 1 and further describes the circuit substrate as a printed circuit substrate.

Claim 11 depends from claim 1 and also describes a passive component 15 which is formed on the transparent substrate and is electrically connected to the circuit for electrical inter-connection.

Claim 12 depends from claim 1 and further describes an active component 16 which is formed on the transparent substrate and electrically connects it to the circuit for electrical inter-connection.

Independent claim 13 describes an integrated module having a transparent substrate 11, which has a circuit layer 110 formed directly on one surface. The circuit layer includes a circuit for electrical inter-connection 111. A plurality of second bumps 114 are formed on part of the

circuit for electrical inter-connection. At least two chips are connected to bumps on the circuit for electrical inter-connection by way of flip-chip bonding. The chips and the circuit for electrical inter-connection form the circuit system.

Claim 14 depends from claim 13 and further describes the circuit layer as including a plurality of electrical pads 112 and a plurality of first bumps 113 formed on the pads.

Claim 15 depends from claim 13 and further describes the transparent substrate as a glass substrate (Paragraph [0012]).

Claim 16 depends from claim 13 and describes the second bumps as being solder bumps or gold bumps.

Claim 19 depends from claim 13 and further describes a passive component 15 which is electrically connected to the circuit for electrical inter-connection.

Claim 20 depends from claim 13 and describes an active component 16 which is formed on the transparent substrate and electrically connected to the circuit for electrical inter-connection.

Claim 21 is an independent claim previously formed from claim 1 and claim 8. Thus, this claim includes limitations described above in regard to claim 1 and further states that the circuit substrate has a hollow portion 132 and when the circuit substrate is attached to the transparent substrate, the chips are positioned in the hollow portion.

Claim 22 depends from claim 21 and further describes the transparent substrate as a glass substrate(Paragraph [0012]).

Claim 23 depends from claim 21 and further describes a plurality of first bumps 113 formed on the electrical pads of the transparent substrate to connect the electrical pads and the circuit layer of the circuit substrate.

Claim 24 depends from claim 21 and further describes a plurality of second bumps 114 formed on the circuit for electrical inter-connection with the chips being electrically connected to the second bumps by way of a flip-chip bonding.

Claim 25 depends from claim 21 and further describes a heat dissipation element 14 formed on the backside of at least one of the chips.

Claim 26 depends from claim 21 and points out the circuit substrate is a printed circuit substrate(Paragraph [0033]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4, 9-16 and 19-26 stand rejected under 35 U.S.C. § 103 as being obvious over Takahashi et al. (U.S. Patent No. 5,903,239) in view of Stopperan (U.S. Patent No. 5,719,749).

VII. ARGUMENT

The Examiner has rejected all of the claims as being obvious over Takahashi et al. in view of Stopperan. With regard to claim 1, the Examiner states that Takahashi et al. includes transparent substrate 1a which has a circuit layer formed on one surface. Takahashi et al. does have a substrate 1a which may be glass (*see* column 4, line 41). While glass is often transparent, the specification does not specifically say that this substrate is transparent. More importantly, the Examiner has identified the circuit layer as the microstrip line 8 and antenna 4. However, the substrate 1a is separated from this microstrip arrangement by a ground plane 2a and a dielectric film 3a. The Examiner has also stated in his comments that Takahashi et al. has layer 2a formed directly on the surface of the transparent substrate. However, the claim recites that the chips form a circuit system with the circuit for electrical inter-connection which is part of the circuit layer. The chips in Takahashi et al. are not connected to the ground conductor film 2a and in fact cannot be connected thereto in order to operate properly. The ground plane prevents electrical signals from being transmitted to anything connected thereto. Furthermore, the chips are separated from the ground plane by the dielectric film specifically so that contact cannot be

made. The claim also recites a plurality of electrical pads. The Examiner has identified this element in the reference by numeral 4, which is the antenna. Applicants do not see the relevance of this element as an electrical pad. However, it is assumed that the Examiner meant that the pads are the ends of the microstrip line 7 and 8. The Examiner also admits that the Takahashi et al. reference does not show a circuit substrate attached to the transparent substrate.

The Examiner cited Stopperan to show a circuit substrate 40 which is attached to a transparent substrate. It is assumed that the Examiner is referring to printed circuit board 20 as the transparent substrate. The reference indicates that layer 22 which is the base for substrate 20 may be made of a number of different materials as discussed at column 4, lines 27-37. The reference does not identify any of these materials as being transparent. Furthermore, Applicant submits that while this reference does show the mounting of an overlay 40 on a printed circuit board 20 using bonding pads 36, the other details of the circuit substrate and transparent substrate are not seen as suggested by the Examiner. Furthermore, it is noted that a chip 70 is provided on overlay 40, which the Examiner equates to the circuit substrate while in the claim, the chips are connected to the transparent substrate.

Applicant submits that even if these references are taken together, they still do not teach the present invention and that the invention of claim 1 would not be obvious thereover. At best, Stopperan only teaches the mounting of one substrate on a printed circuit board. Even if the substrate of Takahashi et al. is mounted on a printed circuit board or other substrate as taught by Stopperan, there still would be no teaching of the use of transparent substrates nor of the circuit layer formed directly on one surface of the transparent substrate. Accordingly, Applicant submits that claim 1 is not obvious over either of these references or their combination.

Claim 2 depends from claim 1 and as such is also allowable. In addition, this claim describes the transparent substrate as being glass.

Claim 3 depends from claim 1 and describes a plurality of first bumps formed on the electrical pads. The Examiner has equated these bumps to bump 6a of Takahashi et al. However, the bumps are stated to be formed on electrical pads which are not shown in Takahashi

et al. as described above. Further, the bumps are stated to connect the pads of the circuit layer on the transparent substrate to the circuit layer of the circuit substrate. In Takahashi et al., bump 6a connects the chips to the circuit layer of the substrate. Accordingly, Applicant submits that this claim is additionally allowable.

Claim 4 depends from claim 1 and also describes the plurality of second bumps which are connected to the chips by way of a flip-chip bonding. The Examiner has equated these bumps to bumps 6b in Takahashi et al. However, this claim remains allowable based on its dependency from allowable claim 1.

Claim 9 depends from claim 1 and further describes a heat dissipation element formed on the backside of at least one of the chips. The Examiner has merely stated that this would be obvious since heat dissipation elements are well known. Applicant submits that the Examiner has not met his burden of showing this feature.

Claim 10 depends from claim 1 and further describes a circuit substrate as a printed circuit substrate. This claim remains allowable based on its dependency from allowable claim 1.

Claims 11 and 12 depend from claim 1 and also describe either a passive component or an active component found on the transparent substrate and electrically connected to the circuit for electrical inter-connection. The Examiner states that Takahashi et al. teaches this feature at Col. 7, lines 49-53. It is noted that this is the final paragraph of the specification and only says that the detection circuit which is an active circuit and the base chip or the antenna chip, which are passive circuits are formed through different processings. It does not state that active components and active components can be formed on the transparent substrate and electrically connected to the circuit for electrical inter-connection.

Claim 13 is an independent claim which includes a number of the limitations of claim 1. Thus, this claim includes the same description of the transparent substrate, the circuit layer formed directly on the surface of the transparent substrate and where the circuit layer includes a circuit for electrical inter-connection. The claim also describes two chips electrically connected

to the electrical inter-connection by flip-chip bonding which form a circuit system. Applicant submits that claim 13 is allowable for the same reasons recited in regard to claim 1 concerning the lack of a transparent substrate on Takahashi et al. which has a circuit layer formed on the surface and on which the two chips are connected.

It should be noted that claim 13 does not include the language regarding the electrical pads that are found in claim 1 but does describe the plurality of second bumps to which the chips are connected. Claim 13 also does not describe the circuit substrate. However, Applicant submits that claim 13 remains allowable since the Takahashi et al. reference does not show the circuit layer formed on the transparent substrate as described above, but instead has a substrate which is separated from any circuit layer by a ground plane 2a and a dielectric film 3a. Accordingly, Applicant submits that claim 13 is likewise allowable.

Claim 14 depends from claim 13 and also further describes the electrical pads and the plurality of first bumps formed on the electrical pads. Claim 14 is similar to claim 3 and is also allowable for the reasons presented there. Takahashi et al. does not show a plurality of electrical pads for electrical external connection. Accordingly, Applicant submits that claim 14 is additionally allowable.

Claim 15 depends from claim 13 and also describes the transparent substrate as being glass. This claim corresponds to claim 2 and remains allowable based on its dependency from allowable claim 13.

Claim 16 depends from claim 13 and describes the second bumps as being solder bumps or gold bumps. Applicant submits that this claim remains allowable based on its dependency from allowable claim 13.

Claims 19 and 20 describe a passive component and an active component, respectively and correspond to claims 11 and 12. Applicant submits that these claims are additionally allowable for the reasons presented above in regard to claims 11 and 12.

Claim 21 is an independent claim which was previously formed from a combination of claim 1 and canceled claim 8. Thus, claim 21 is allowable for all the reasons recited above with regard to claim 1 since it includes all of that language. In addition, claim 21 describes that the circuit substrate has a hollow portion and that the circuit substrate is attached to the transparent substrate and the chips are positioned in the hollow portion of the circuit substrate. The Examiner has pointed out in regard to claim 8 that Takahashi et al. does show a hollow portion. This is seen in Figure 8 as a depression in the dielectric substrate and a chip 52 is mounted therein. Applicant submits that this arrangement does not meet the terms of claim 21. That is, the hollow area is formed in the transparent substrate, rather than the circuit substrate as is claimed. The claim also states that the chips are connected to the transparent substrate but positioned in the hollow portion of the circuit substrate. This arrangement is not seen at all in this reference. This can be seen in the present application in Figure 1a where the chips are mounted on the bottom of glass substrate 11 and are positioned in the space between the two parts of circuit substrate 13 show in that Figure. Therefore, Applicant submits that claim 21 is further allowable.

Claim 22 depends from claim 21 and further describes the transparent substrate as being glass. This corresponds to claims 2 and 15 and remains allowable based on its dependency from allowable claim 21.

Claim 23 depends from claim 21 and further describes the plurality of first bumps formed on the electrical pads of the transparent substrate. This corresponds to claim 3 and is allowable for the reasons presented there.

Claim 24 depends from claim 21 and further describes the plurality of second bumps. This corresponds to claim 4 and is allowable for the reasons presented there.

Claim 25 depends from claim 21 and further describes the heat dissipation element. This corresponds to claim 9 and is allowable for the reasons presented there.

Claim 26 depends from claim 21 and corresponds to claim 10. This claim is also allowable for the reasons presented there.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

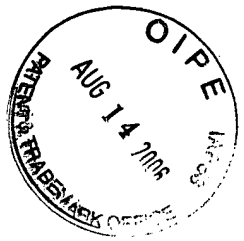
CONCLUSION

In view of the above, Applicant submits that the rejection by the Examiner is in error and should be reversed.

Dated: August 14, 2006

Respectfully submitted,

By _____
Joe McKinney Muncy
Registration No.: 32,334
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant



APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/648,253

1. A multi-chip integrated module, comprising:

a transparent substrate, which has a circuit layer formed directly on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate comprises a circuit for electrical inter-connection and a plurality of electrical pads;

at least two chips, which are respectively mounted on the transparent substrate by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system; and

a circuit substrate, which attaches to the transparent substrate, and at least comprises a circuit layer of the circuit substrate, wherein the electrical pads of the transparent substrate electrically connect to the circuit layer of the circuit substrate.

2. The multi-chip integrated module of claim 1, wherein the transparent substrate is a glass substrate.

3. The multi-chip integrated module of claim 1, wherein a plurality of first bumps are formed on the electrical pads of the transparent substrate, respectively, for electrically connecting the electrical pads and the circuit layer of the circuit substrate.

4. The multi-chip integrated module of claim 1, wherein a plurality of second bumps are formed on a part of the circuit for electrical inter-connection, and the chips electrically connect to the second bumps by way of a flip-chip bonding.

9. The multi-chip integrated module of claim 8, wherein a heat dissipation element is formed on the backside of at least one of the chips.

10. The multi-chip integrated module of claim 1, wherein the circuit substrate is a printed circuit substrate.

11. The multi-chip integrated module of claim 1, further comprising:

a passive component, which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

12. The multi-chip integrated module of claim 1, further comprising:

an active component, which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

13. A multi-chip integrated module, comprising:

a transparent substrate, which has a circuit layer formed directly on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate

comprises a circuit for electrical inter-connection, and a plurality of second bumps are formed on a part of the circuit for electrical inter-connection; and

at least two chips, which electrically connect to the bumps of the circuit for electrical inter-connection by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system.

14. The multi-chip integrated module of claim 13, wherein the circuit layer of the transparent substrate further comprises a plurality of electrical pads for electrical external-connection, and a plurality of first bumps are formed on the electrical pads, respectively.

15. The multi-chip integrated module of claim 13, wherein the transparent substrate is a glass substrate.

16. The multi-chip integrated module of claim 13, wherein the second bumps are solder bumps or gold bumps.

19. The multi-chip integrated module of claim 13, further comprising:
a passive component, which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

20. The multi-chip integrated module of claim 13, further comprising:

an active component, which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate.

21. A multi-chip integrated module, comprising:

a transparent substrate, which has a circuit layer formed directly on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate comprises a circuit for electrical inter-connection and a plurality of electrical pads;

at least two chips, which are respectively mounted on the transparent substrate by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system; and

a circuit substrate, which attaches to the transparent substrate, and at least comprises a circuit layer of the circuit substrate, wherein the electrical pads of the transparent substrate electrically connect to the circuit layer of the circuit substrate, the circuit substrate has a hollow portion, and when the circuit substrate attaches to the transparent substrate, the chips are positioned in the hollow portion of the circuit substrate.

22. The multi-chip integrated module of claim 21, wherein the transparent substrate is a glass substrate.

23. The multi-chip integrated module of claim 21, wherein a plurality of first bumps are formed on the electrical pads of the transparent substrate, respectively, for electrically connecting the electrical pads and the circuit layer of the circuit substrate.

24. The multi-chip integrated module of claim 21, wherein a plurality of second bumps are formed on a part of the circuit for electrical inter-connection, and the chips electrically connect to the second bumps by way of a flip-chip bonding.

25. The multi-chip integrated module of claim 21, wherein a heat dissipation element is formed on the backside of at least one of the chips.

26. The multi-chip integrated module of claim 21, wherein the circuit substrate is a printed circuit substrate.

EVIDENCE APPENDIX B

IX. No evidence is being submitted.

RELATED PROCEEDINGS APPENDIX C

X. There are no related proceedings.